

REMARKS

Regarding paragraph 1 of the Office Action, it makes reference to two patents which are respectively cited on line 1 of page 4 and line 17 of page 43 in the present patent application. But, the first patent 6,307,391 (which is cited on page 4) is listed as item B on form PTO-892. Similarly, the second patent 4,415,409 (which is cited on page 43) also is listed on form PTO-892 as item D. This indicates that the relevance of the '391 patent and the '409 patent, to teaching the present invention as claimed, has been considered by the Office.

Next, regarding paragraph 2 of the Office Action, it says that the drawings fail to comply with 37CFR1.84(p)(5) because items 81-85 are shown in Figs. 1, 9-11, and 14; but those items are "not mentioned in the description". However, the above position is without merit. All of the items 81-85 are described in the specification at lines 19-29 on page 15.

Next, regarding paragraphs 3-5 of the Office Action, they all indicate that "numerous pages" of the Detailed Description and "claim 2" have words with missing letters. Accordingly, the undersigned attorney made the following checks on his copy of the present patent application: 1) looked for missing letters in the words on each page of the Detailed Description, and 2) looked for missing letters in each claim. However, no missing letters were found. For example, no "e" is missing from "wherein" in line 1 of claim 2, as stated in the Office Action.

In an effort to solve the above puzzle, the undersigned attorney called Examiner Hollington and thereby determined that the Examiner was not working from the paper

copy of the present application which was originally mailed to the USPTO, but instead was working from a copy that had been optically scanned into his PC. The original paper copy of the present application that was mailed to the USPTO should contain no missing letters since it is a "Xerox" of the application which is in the file of the undersigned attorney. This indicates that a scanning error occurred in the USPTO. Accordingly, Examiner Hollington agreed to try to locate the original paper copy of the present application as mailed to the USPTO and have it re-scanned into his PC.

Next, regarding paragraphs 6-7 of the Office Action, they reject claim 1-5 and 7-12 under 35USC102(b) as being "anticipated" by Friedrich et al. (6,307,388). Here, claim 1 is the only independent claim. So if claim 1 is found to be not anticipated by patent `388, then all of claims 1-14 should be allowable.

To support the above rejection of claim 1, the Office Action attempts to correlate the language of claim 1 with various items that are in the `388 patent. This correlation occurs in the paragraph that starts on the bottom of page 3 and ends on the top of page 4. However, that correlation is in error for reasons which will now be pointed out.

In claim 1, a "signal generator" is recited which "sends test signals concurrently to said IC-chips on all chip holding subassemblies that are at said test position, where said test signals are shifted in time from one subassembly to another". An example of these time shifted test signals from the signal generator is seen in Fig. 7A. There, at time t2, the signal generator starts to send test signals to the IC-chips that are in the subassembly 21.

Later, at time t4, the signal generator starts to send test signals to the IC-chips that are in the subassembly 22. Still later, at time t6, the signal generator starts to send test signals to the IC-chips that in the subassembly 23. Even later, at time t8, the signal generator starts to send test signals to the IC-chips that in the subassembly 24.

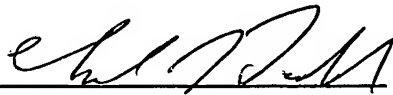
By comparison, in patent `388, the test signals are not shifted in time from one chip holding subassembly to another. Instead in patent `388, all of the chip holding subassemblies are sent the same test signals at the same time. This occurs in patent `388 because there, all of the chip holding subassemblies are moved from the "open" position to the "closed" position (which is where the chips are tested) at the same time.

In patent `388, Fig. 1A shows a motor 16c which moves two levers 16d and 16c simultaneously, and those levers move two plates 16a and 16b simultaneously. Plate 16a has one respective pair of holes 16a-1 for each of the chip holding subassemblies 12, and plate 16b has another respective pair of holes 16b-1 for each of the chip holding subassemblies 12. As the plates 16a and 16b move, their holes 16a-1 and 16b-1 move the ends 15e of a respective set of arms 15b. These arms move from an "open" position to a "closed" position and visa-versa as shown in Fig. 2, for all of the chip holding subassemblies 12 at the same time. In the "open" position, chips are unloaded/loaded into all of the subassemblies 12. In the closed position, the chips in all of the subassemblies 12 are tested at the same time by the same test signals which are labeled "SIGNALS" in Fig. 2.

A major problem with the above system of patent '388 is that while all of the chip holding subassemblies are at the "open" position, the system is not being utilized to actually test any IC-chips. By comparison, with the system of the present claim 1, this utilization problem is overcome. This is illustrated in Fig. 7B wherein at any one particular time instant t9-t16, at least three of the four chip holding subassemblies 21-24 are actually testing IC-chips by receiving test signals that are shifted in time from one subassembly to another.

Based on the above REMARKS, all grounds for rejection in the last Office Action should now be overcome. Accordingly, an early Notice of Allowance of all of the claims 1-14 is requested.

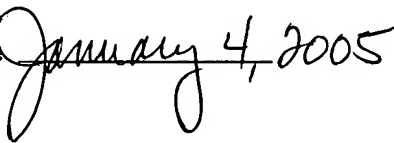
Respectfully submitted,

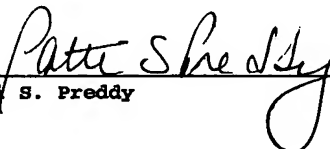
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Patti S. Preddy